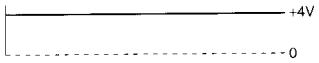
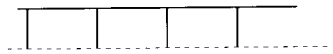
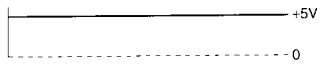
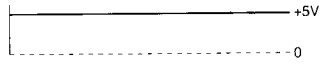
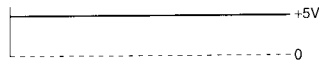
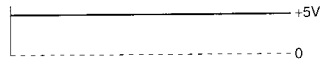
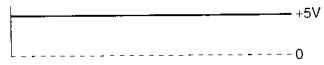
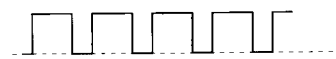
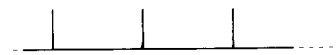
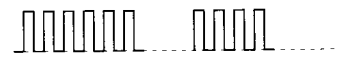
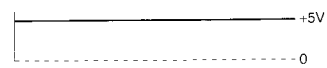
| Comp | Name (pin) Circ /IC | Scope | Freq. Per. | Data H/L/A | Description |
|---|---|---|---|---|---|
| 19 | /ACH2 |   | 0 | H | /Analog channel 2 |
| 20 | /ACH6 |   | 0 | H | /Analog channel 6 |
| 21 | /ACH7 |  | 0 | A | /Analog channel 7 |
| 22 | /VSS |  | 0 | L | /Voltage supply ground (0) |
| 23 | /ACH5 |  | 0 | L | /Analog channel 5 |
| 24 | HLDOFN/ACH4 |  | | H | /A Hold off not /Analog channel 4 |
| 25 | /ANGND |  | 0 | L | /Analog ground (A/D convertor) |
| 26 | /VREF |   | 0 | H | /Vreference (A/D convertor) |
| 27 | /VSS |  | 0 | L | /Clock Detect Enable |
| 28 | ACQRDY/EXTINT |  | ≈50 Hz | A | Acquisition ready/External interrupt |
| 29 | /VCC |   | 0 | H | /Main supply (+5V) |
| 30 | µPRESET/$\overline{\text{RESET}}$ |   | 0 | H | µP reset /reset |
| 31 | /RXD |   | 0 | H | /Receive data/port 2 |
| 32 | /TXD |   | 0 | H | /Transmit data/port 2 |
| 33 | /VSS |  | 0 | L | /Voltage supply ground (0) |
| 34 | CDAT /P1.0 |  | ≈20 µs | A | Cbus DATA /Port 1.0; repeated each 30-60 ms |
| 35 | DTAEb/P1.1 |  | 30-60 ms | L | DATA enable /Port 1.1 |
| 36 | FRONTCLOCK/P1.2 |  | 60 kHz | A | Front clock /Port 1.2; repeated each 30-60 ms |
| 37 | CCLK /P1.3 |  | 100 kHz | A | Cbus clock /Port 1.3; repeated each 30-60 ms |
| 38 | PS0 /P1.4 |  | 40 Hz | A | page select 0 /Port 1.4 |
| 39 | FRONTDATA1/HS1.0 |   | 0 | H | Frontdata1 /High speed input 1.0 |